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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/864,725	05/23/2001	Shirish Gadre	SONY-50P4107	2789

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EXAMINER	
NGUYEN, MIKE	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 02/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/864,725	GADRE ET AL.	
	Examiner	Art Unit	
	Mike Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Notices & Remarks

1. Claims 1-27 are pending for the examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims are 1-3, 5-6, 8, 10-13, 15, 17, 19-21, 23, 25 and 27 rejected under 35 U.S.C. 102(b) as being anticipated by Hori (U.S. Pat. No. 5,943,509).

As to claim 1, Hori teaches a data and communication apparatus communicatively coupled with a multi-processor shared memory multimedia chip system for providing interprocessor communication while enhancing performance of each processor integral with said multi-processor shared memory multimedia chip system (fig. 2 col. 3 lines 46-55), said data and communication apparatus comprising:

a data memory to retrievably store data (selector 34a col. 4 lines 18-28);

an instruction memory coupled with said data memory to retrievably store instructions (request circuits 38-1, 2 3 and notification circuits 39-1, 2, 3 col. 4 lines 1-18);

an incoming buffer (FIFO 34 or FIFO 36) coupled with said data memory and said instruction memory which permits transfer of data into said data and communication apparatus (col. 3 lines 62-67), said incoming buffer further adapted to provide fast access to streaming data (col. 4 line 38 to col. 6 line 19); and

an outgoing buffer (output circuit 34b or 34c) coupled with said data memory and instruction memory which monitors and permits transfer of data out of said data and communication apparatus (fig. 2 col. 4 lines 19-34), said outgoing buffer enables said each processor to communicate with other processors disposed within said system (col. 4 lines 38-46 and col. 5 lines 36-45).

As to claims 2, 11 and 27, Hori teaches multiple registers (registers 36, 37) coupled with said data and communication apparatus, said registers adapted to provide enhanced configurability and control of said data and communication apparatus, said register further adapted to provide addressable memory storage locations for said retrievably stored data and said retrievable stored instruction, said registers separate from and in addition to the registers within said multi-processor shared memory multimedia chip system (col. 3 lines 62-67).

As to claims 3 and 12, Hori teaches said data and communication apparatus is coupled with said multi-processor shared memory multimedia chip system (fig. 2), wherein access to said data and communication apparatus is via an I/O space (bus) (DB2, DB3), said I/O space (bus) separate from a memory space (bus) of said device (AB2, AB3), said I/O space pre-existent within said system (col. 3 lines 46-61).

As to claims 4, 13 and 21, Hori teaches said data said retrievably stored in said data memory is an interrupt service routine, wherein access to retrieve said interrupt service routine is

via said I/O space, such that traffic on said memory space is commensurately reduced, so as to ensure the time required to complete said interrupt service routine (col. 5 lines 4-35).

As to claims 6, 15 and 24, Hori teaches said instructions said retrievably stored in said instruction memory are a function of a particular process, said function having certain tendencies relative to said particular process, wherein after said particular process is completed, said function of said particular process is removed, such that a subsequent function of a subsequent process is then stored in said instruction memory unit (col. 5 lines 10-25 and col. 6 lines 6-19).

As to claims 8,17 and 25, Hori teaches said outgoing buffer enables said a processor of said multi-processor multimedia chip system to send said communications to other processors disposed within said multi-processor multimedia chip system while independently processing other tasks, such that said processing of said other tasks in not disrupted (col. 4 lines 19-34 and col. 4 lines 42-46 and col. 5 lines 40-45).

As to claim 10, Hori teaches a multi-processor shared memory multimedia chip system having a data and communication apparatus coupled with said multi-processor shared memory multimedia chip system, said data and communication apparatus for providing interprocessor communication while enhancing performance of each processor integral with said multi-processor shared memory multimedia chip system (fig. 2 col. 3 lines 46-55), said data and communication apparatus comprising:

a data memory to retrievably store data (selector 34a col. 4 lines 18-28);

an instruction memory coupled with said data memory to retrievably store instructions (request circuits 38-1, 2 3 and notification circuits 39-1, 2, 3 col. 4 lines 1-18);

an incoming buffer (FIFO 34 or FIFO 36) coupled with said data memory and said instruction memory which permits transfer of data into said data and communication apparatus (col. 3 lines 62-67), said incoming buffer further adapted to provide fast access to streaming data (col. 4 line 38 to col. 6 line 19); and

an outgoing buffer (output circuit 34b or 34c) coupled with said data memory and instruction memory which monitors and permits transfer of data out of said data and communication apparatus (fig. 2 col. 4 lines 19-34), said outgoing buffer enables said each processor to communicate with other processors disposed within said system (col. 4 lines 38-46 and col. 5 lines 36-45).

As to claim 19, Hori teaches in a multi-processor shared memory multimedia chip system (fig. 2) having a memory space (bus) (AB2 and AB3) and an I/O space (bus) (DB2 and DB3), a method to provide interprocessor communication while enhancing processor performance (col. 3 lines 46-55), said method comprising the step of:

providing an data and communication apparatus (line/trunk circuits 3-1, 3-2) adapted to be communicatively coupled to said multi-processor shared memory multimedia chip system, wherein access to said data and communication apparatus is via said I/O space, said data and communication apparatus further adapted enable said interprocessor communication and said enhanced processor performance (col. 3 lines 46-55).

As to claim 20, Hori teaches the method of claim 19 further comprising the step of providing a data memory to retrievably store data (selector 34a col. 4 lines 18-28).

As to claim 23, Hori teaches the method of claim 19 further comprising the step of providing an instruction memory coupled with said data memory to retrievably store instructions (request circuits 38-1, 2 3 and notification circuits 39-1, 2, 3 col. 4 lines 1-18).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5, 14 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hori in view of Slingwine et al. (U.S. Pat. No. 6,219,690 B1).

As to claims 5, 14 and 22, Hori fails to explicitly teach real-time kernel thread context data wherein said access to retrieve said real-time kernel thread context data is via said I/O space, such that traffic on said memory space in commensurately reduced, so as to increase speed with which thread context switch is achieved. Slingwine; however; teaches minimizing processor associated bus traffic and zero overhead data coherency (col. 4 lines 54 to col. 5 line 20). It would have been obvious to a person of ordinary skill in the art to have minimizing processor associated bus traffic and zero overhead data coherency in order to provide reducing bus traffic (col. 4 lines 56) and concurrently reading and/or updating data while maintaining data coherency (col. 5 lines 17-20).

6. Claims 7, 16 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hori in view Moreno et al. (U.S. Pat. No. 6,711,651 B1).

As to claims 7, 16 and 24, Hori fails to explicitly teach a prefetch mechanism for a particular type of data, so as to enable acceleration of the rate of said incoming buffer's decoding and parsing of header information relative to said particular data type, such that the processing time of said particular type of data is reduced. Moreno; however; teaches prefetch mechanism (col. 7 lines 5-25). It would have been obvious to a person of ordinary skill in the art to have the prefetch mechanism in order to provide avoiding long latency cache misses and excessive coherence traffic (col. 1 lines 42-48).

7. Claims 9, 18 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hori in view Garnett et al. (U.S. Pat. No. 6,148,348).

As to claims 9, 18 and 26, Hori fails to explicitly teach monitoring the number of active communications within said system, such that a maximum of active communications is not exceeded, so as to allow additional active communications to be placed within said system when said allowable will not exceed said maximum number. Garnett; however; teaches a bridge control mechanism monitoring operation of the first and second processing sets (claim 14). It would have been obvious to a person of ordinary skill in the art to have the bridge control mechanism in order to provide limiting the impact of an error or to completely recover from an error (col. 1 lines 28-32).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

U.S. Pat. No. 5,841,988 (Chennubhotla et al.)

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Nguyen whose telephone number is 571 272-4153. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 571 272-4146. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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02/11/2005